Collaboration to Deliver Lithography Solutions

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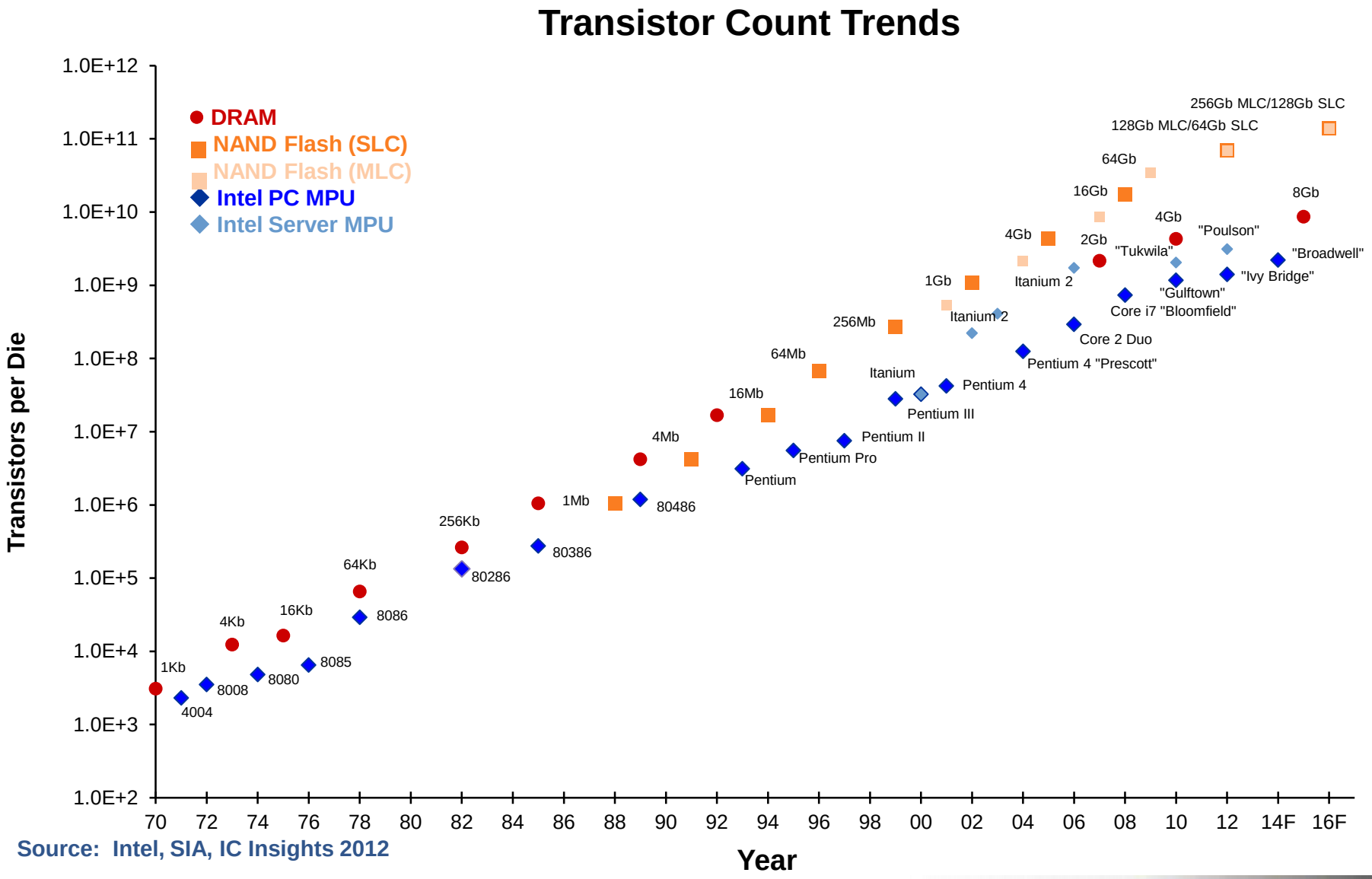
July 10, 2013

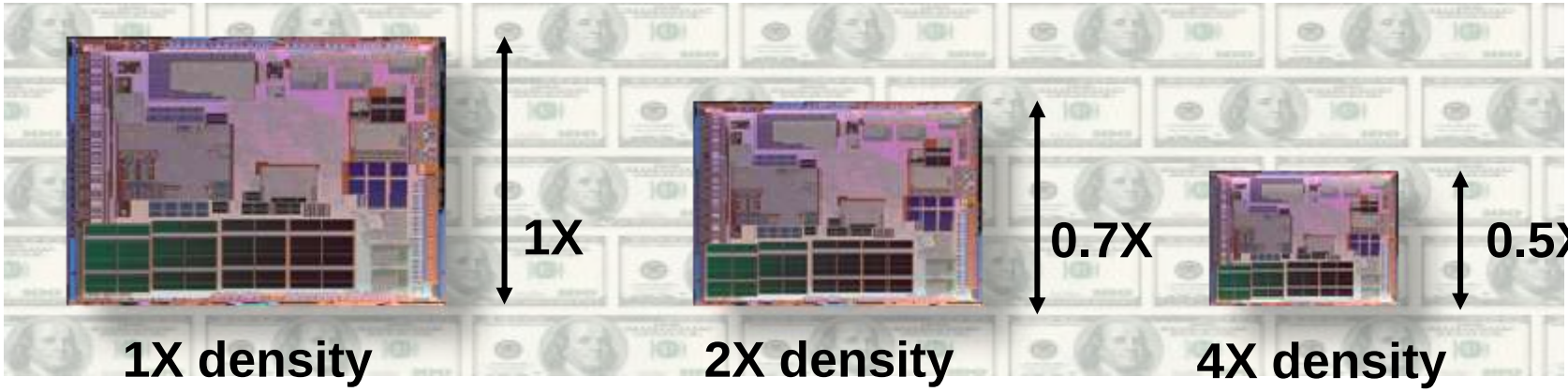
Scaling Continues…



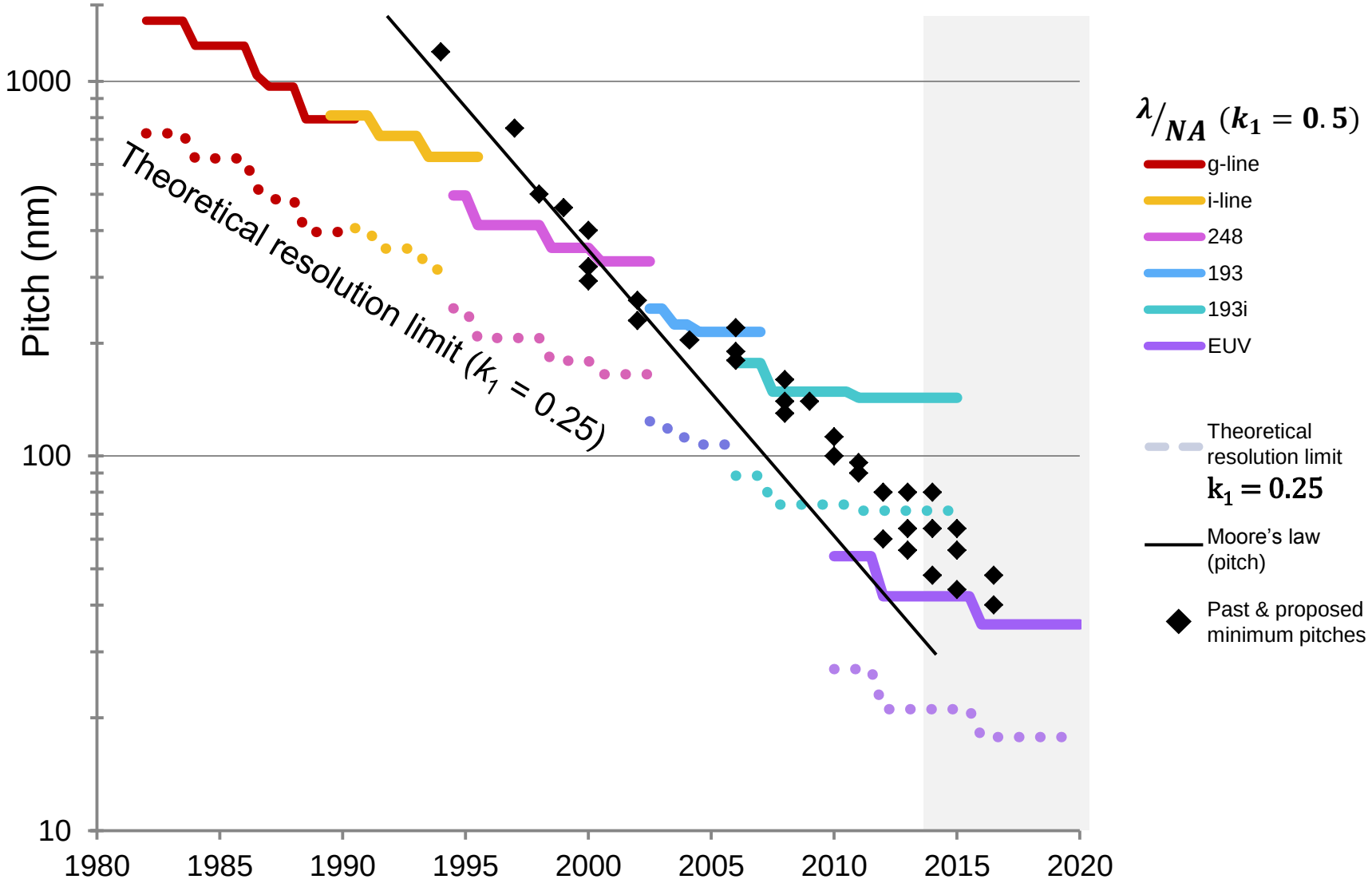
Source: Intel, SIA, IC Insights 2012

Moore's Law is about Number of Components at Minimum Cost

- Lithography's role has been to provide a 70% dimension shrink at every node, thus doubling device density and reducing cost per function.
- With optical lithography at its limits, new materials and complex lithography processes become the drivers for increasing feature density.
- Cost-effective density scaling requires co-optimizing layout design styles with these advanced lithographic processes.

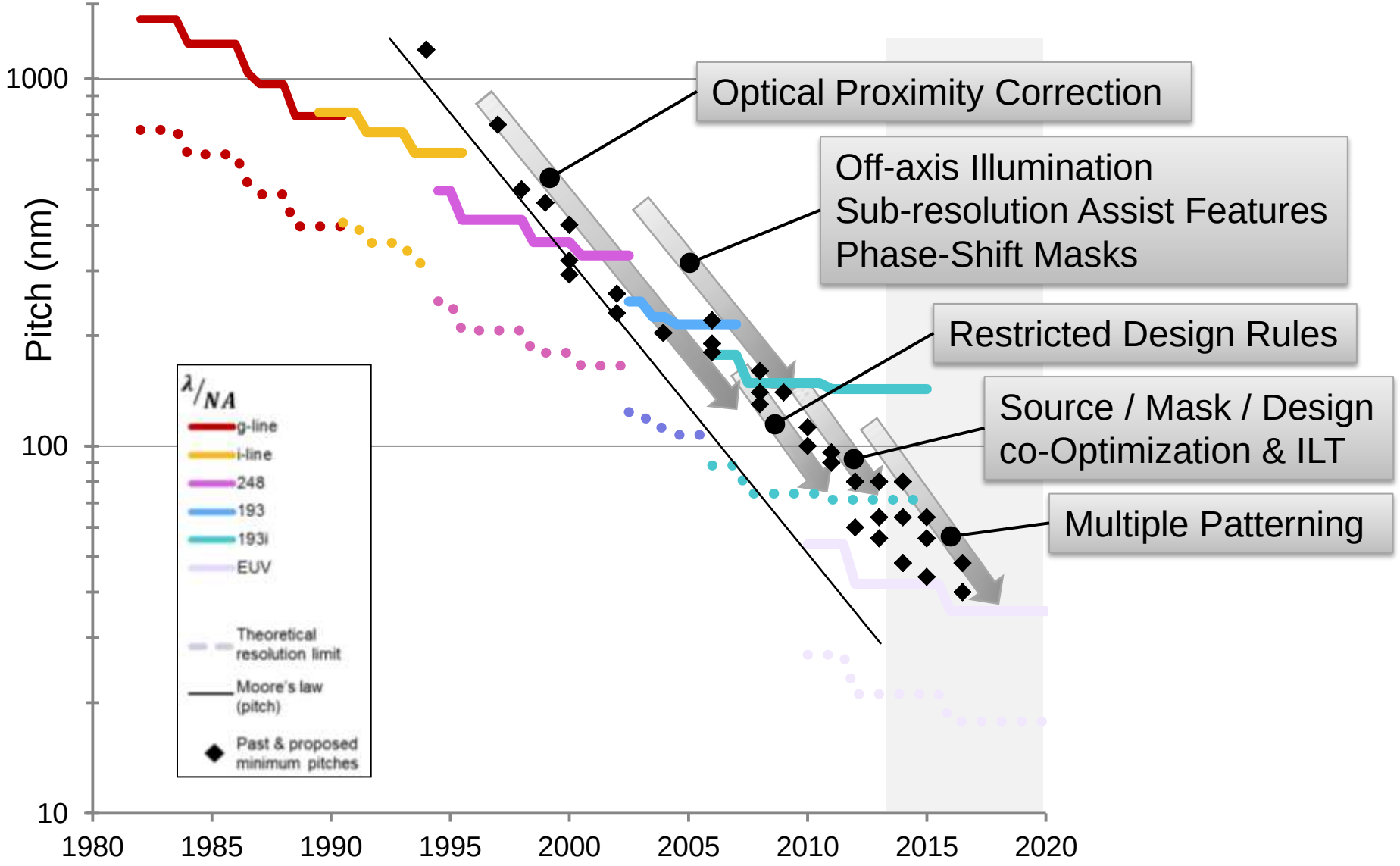


Minimum-Pitch Scaling Trends



M. Rieger, Semicon West, 2013

EDA's Roles to Enable Scaling



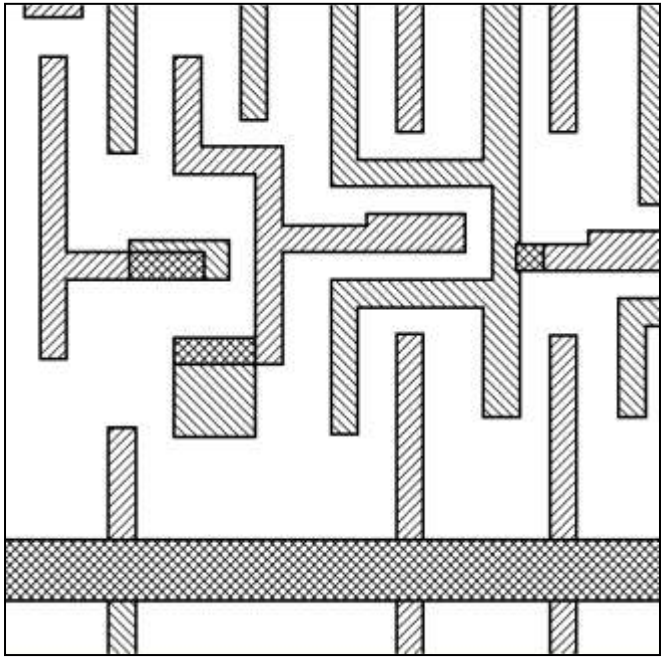
M. Rieger, Semicon West, 2013

Multiple Patterning for Sub-Resolution Pitch

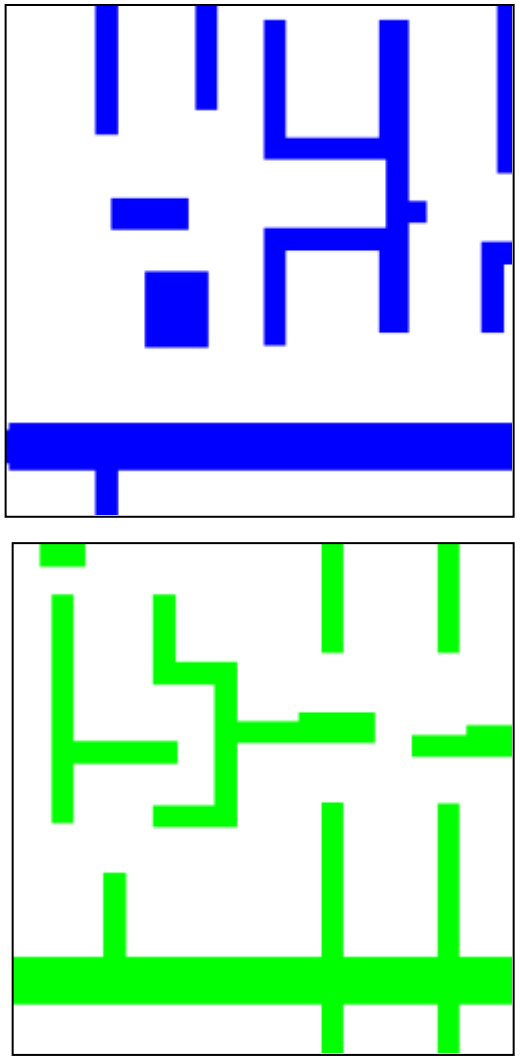
- Pitch Splitting
  - Sort pattern features onto separate sub-pattern masks.
  - Expose and process to fix each sub-pattern in place, one at a time.
    - Litho-etch-litho-etch (LELE)

- Pitch Division (or Frequency Multiplication)
  - Leverage a specialized process to generate multiple features for each exposed feature.
    - Self-aligned (or spacer-assisted) double patterning (SADP).
    - Directed self-assembly (DSA).
  - Practical use requires an additional exposure step to clear out unwanted features.

Pitch Splitting (litho-etch-litho-etch, LELE)

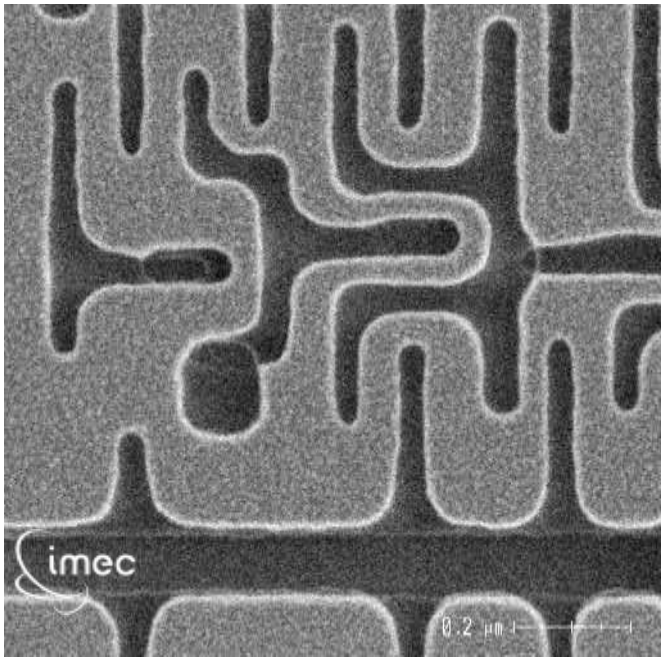


Original pattern



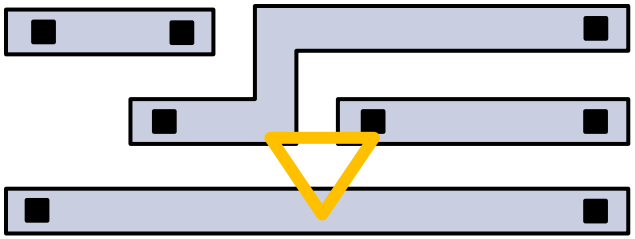
Two masks and exposures with 28nm processing

LELE exposures combined produces final 20nm node wafer pattern

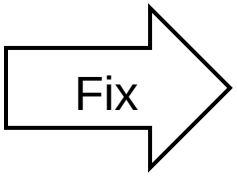


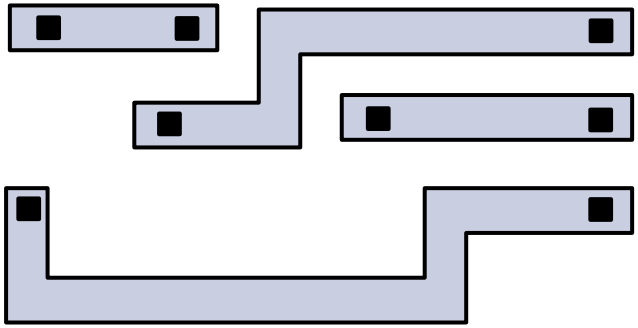
imec

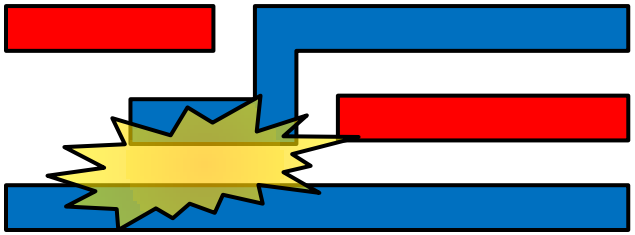
LELE Coloring Constraints



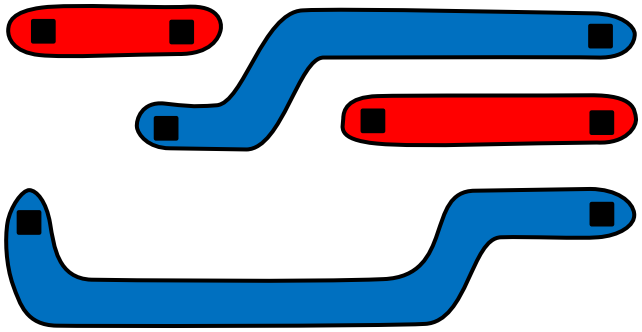
Odd-cycle conflict



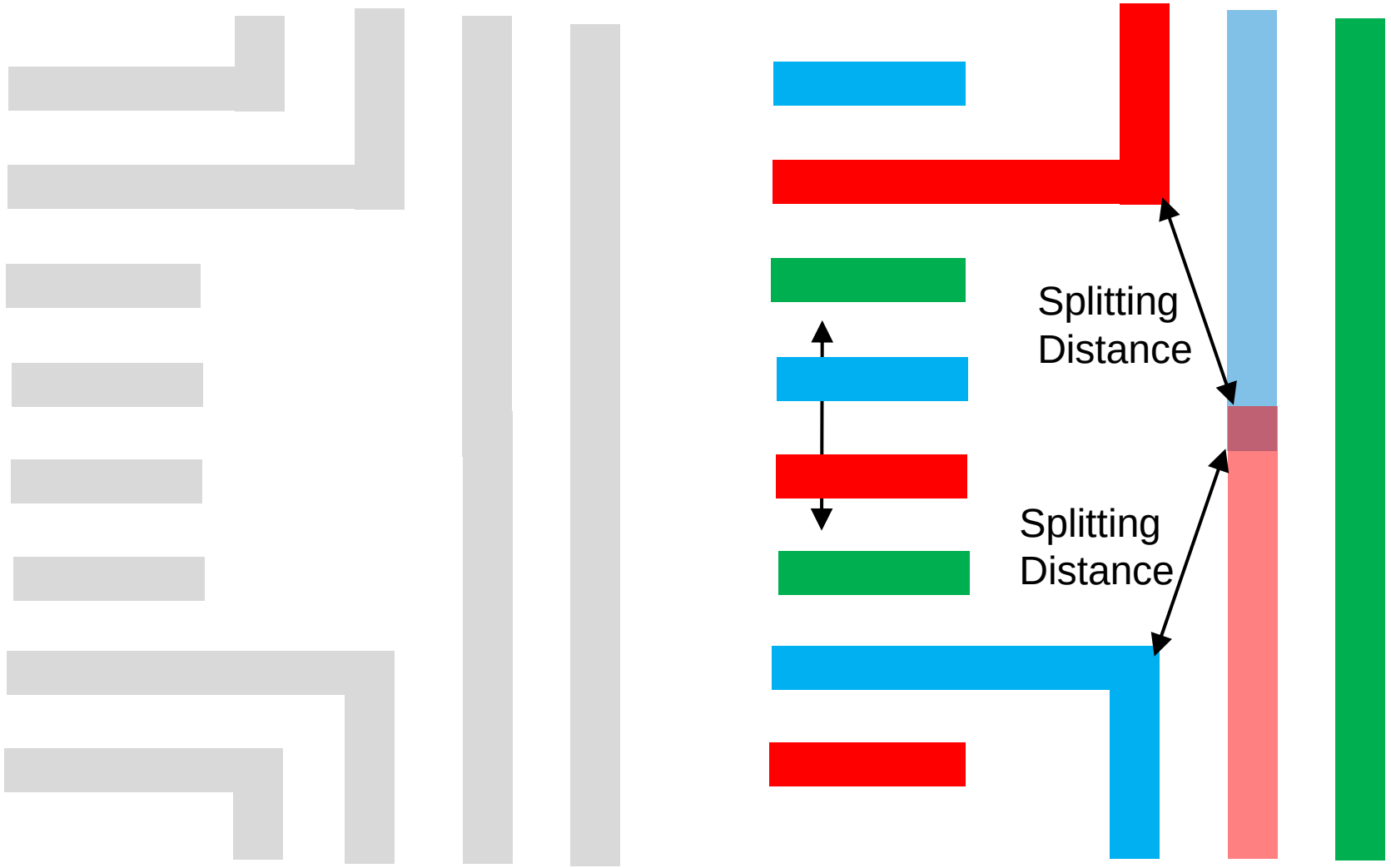




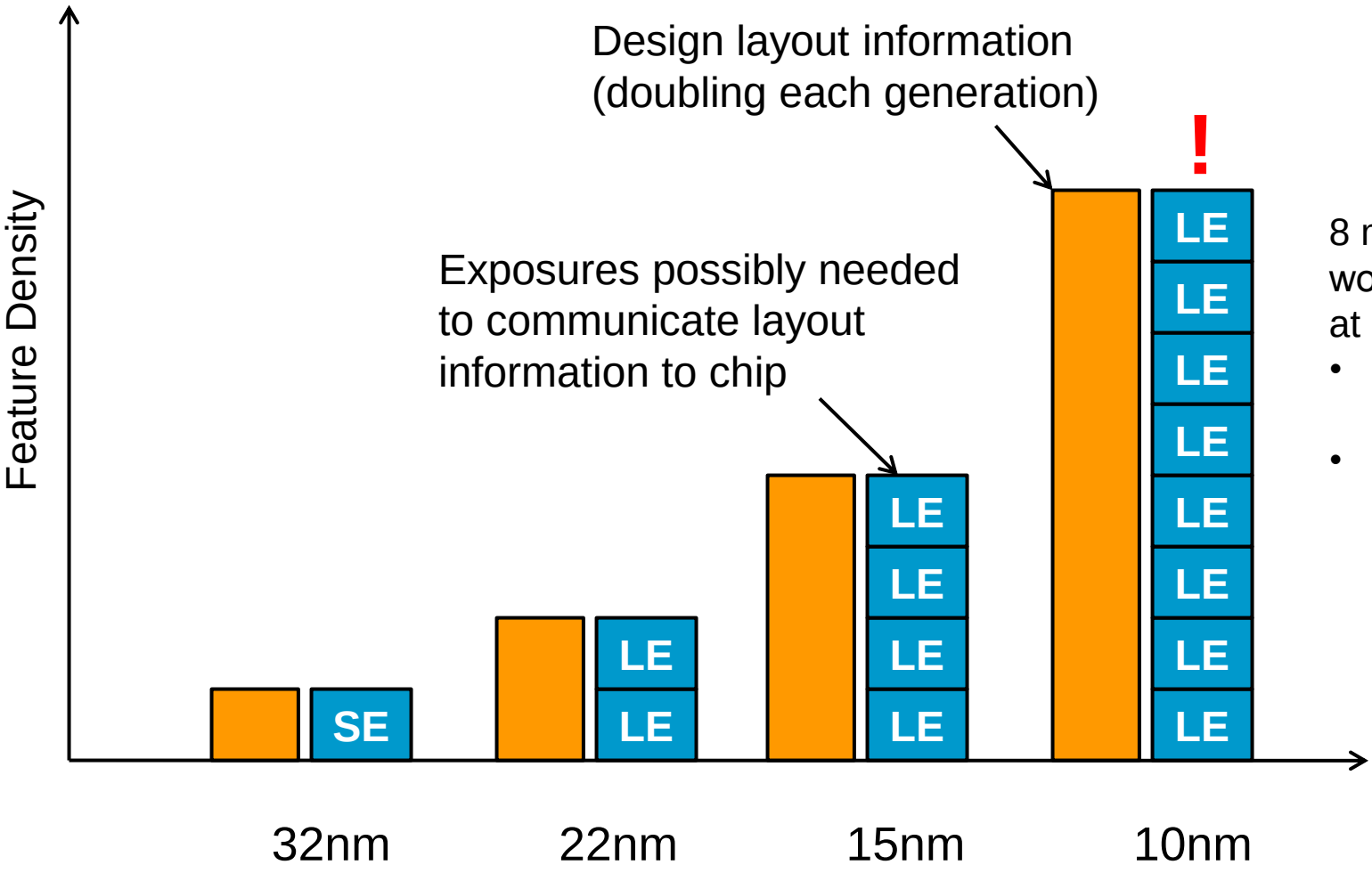
Can’t realize single exposure pattern



Example Triple Splitting (LELELE)



193i LE Exposures Needed for 2X Density per Generation – Without Optimized Layout Styles.



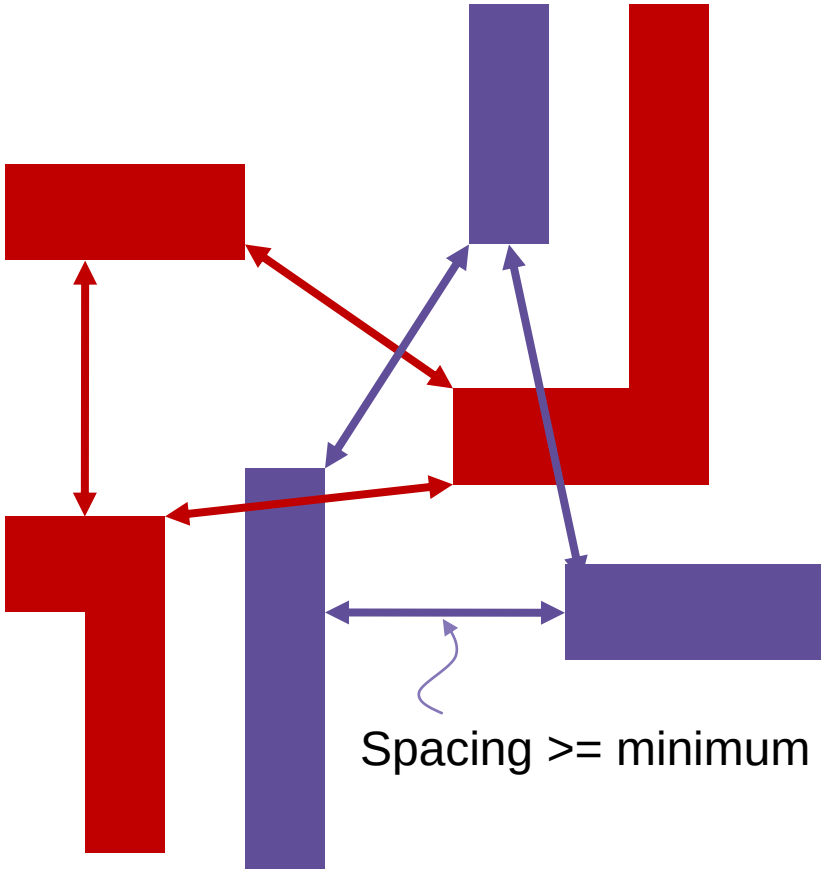
8 masks / layer won't be used at 10nm.

- Pitch is not scaling at 70%/gen.
- 1-D design styles get enhanced pitch scaling with double patterning

SE: Single Exposure
LE: Litho-Etch

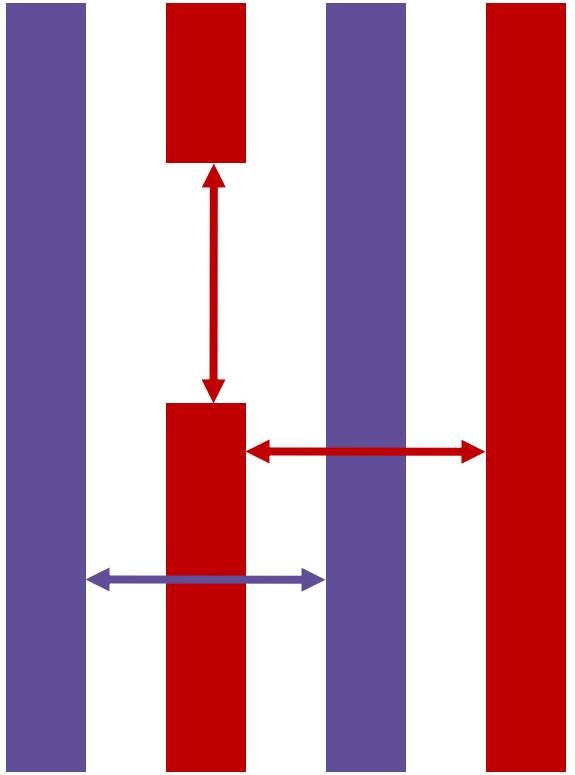
LELE Pattern Pitch

2-D Configurations



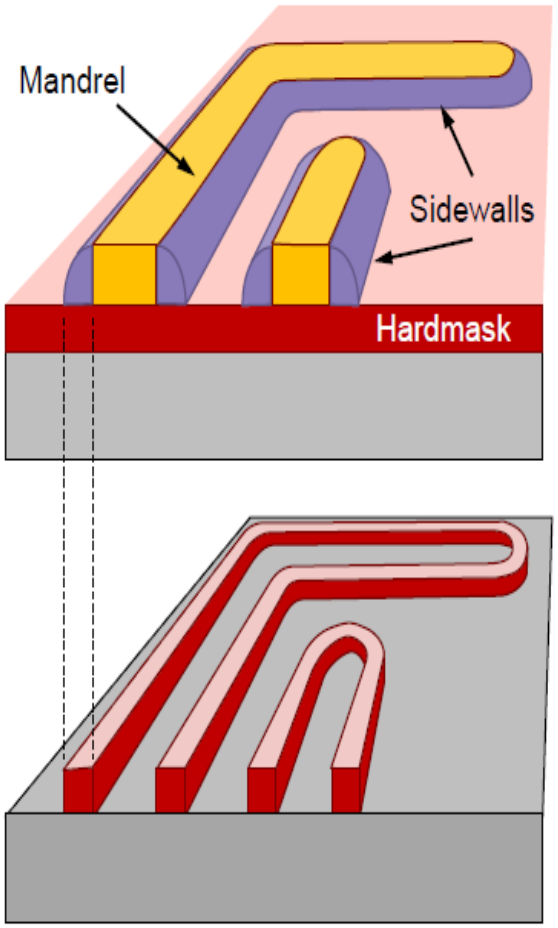
Average pitch scales by ~ 0.7

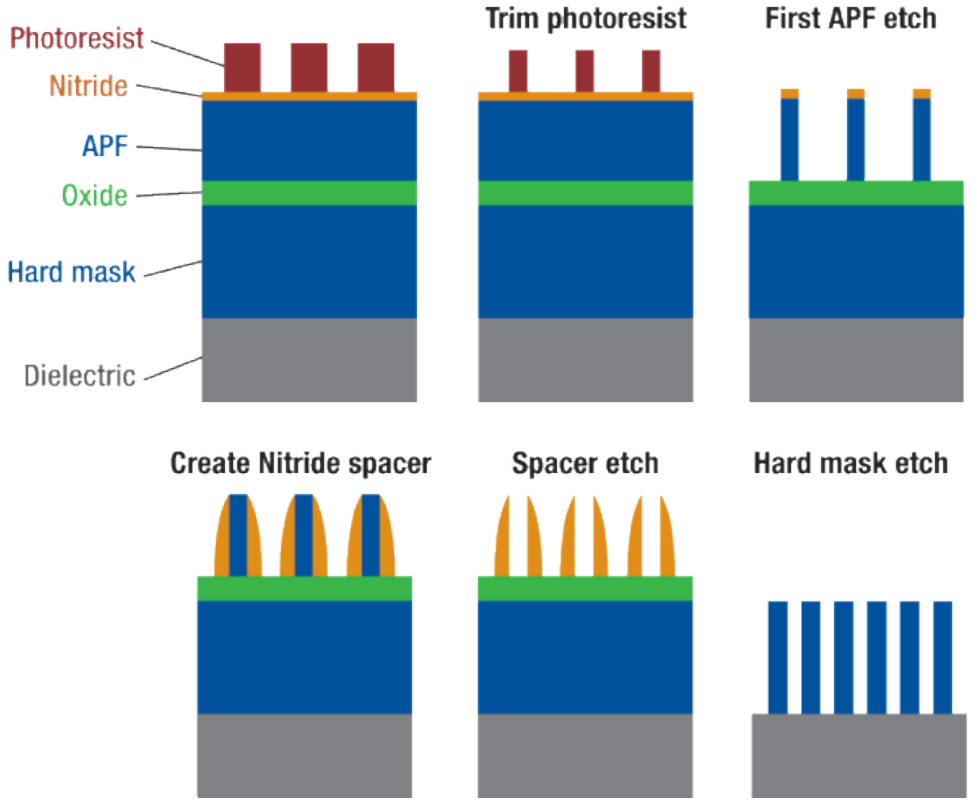
1-D Configurations



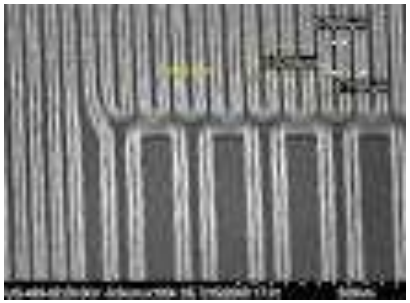
Average pitch scales by ~ 0.5

Pitch Division: Side-Wall Image Transfer (SIT)





O. Montal, Applied Materials
Solid State Technology (2010)

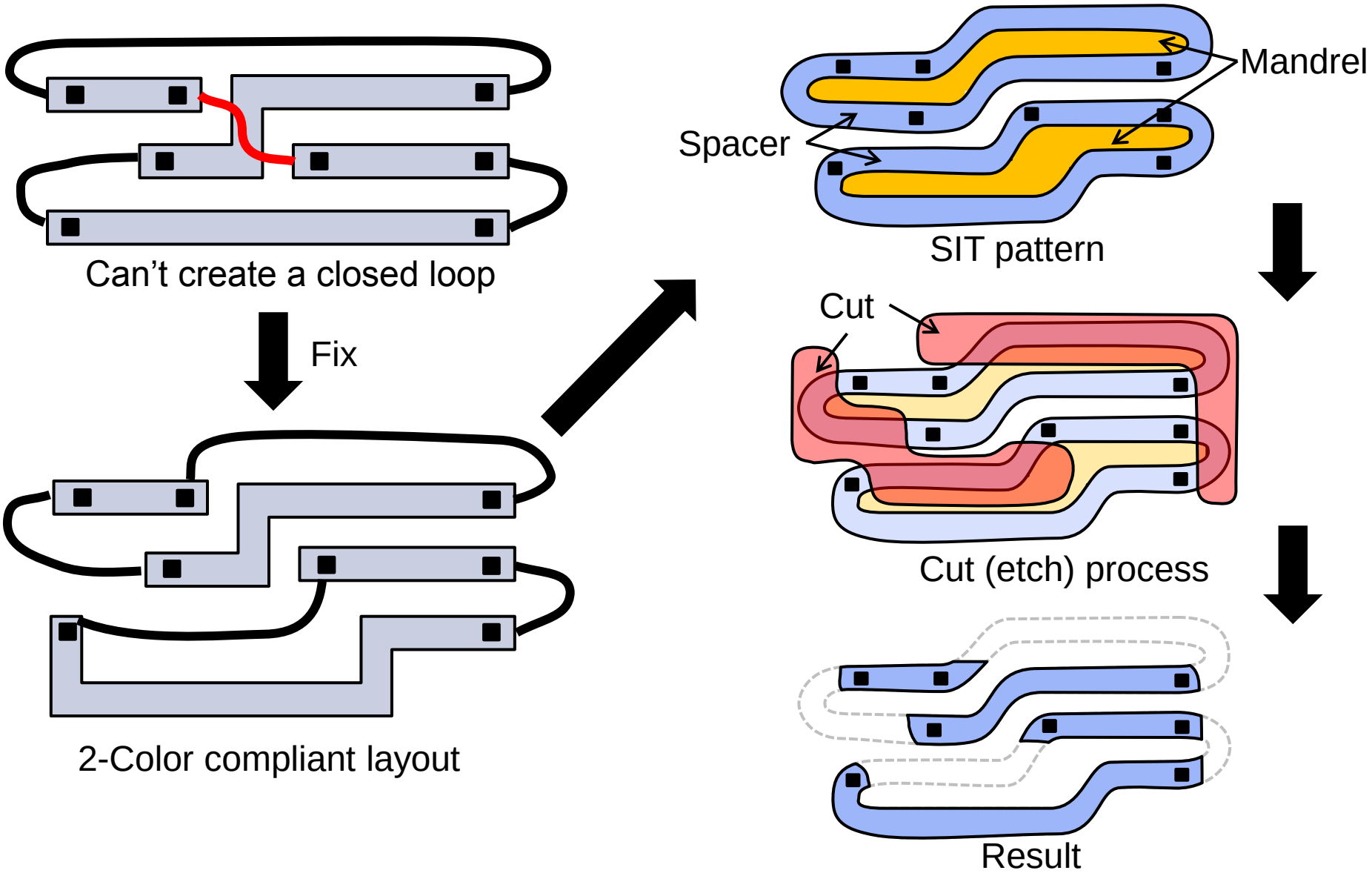


Yan Borodovsky,
Semicon West, 2009

Features are fixed at one process-determined width and always form closed loops.

M. Rieger, Semicon West, 2013

Self-Aligned Double Patterning (SADP)

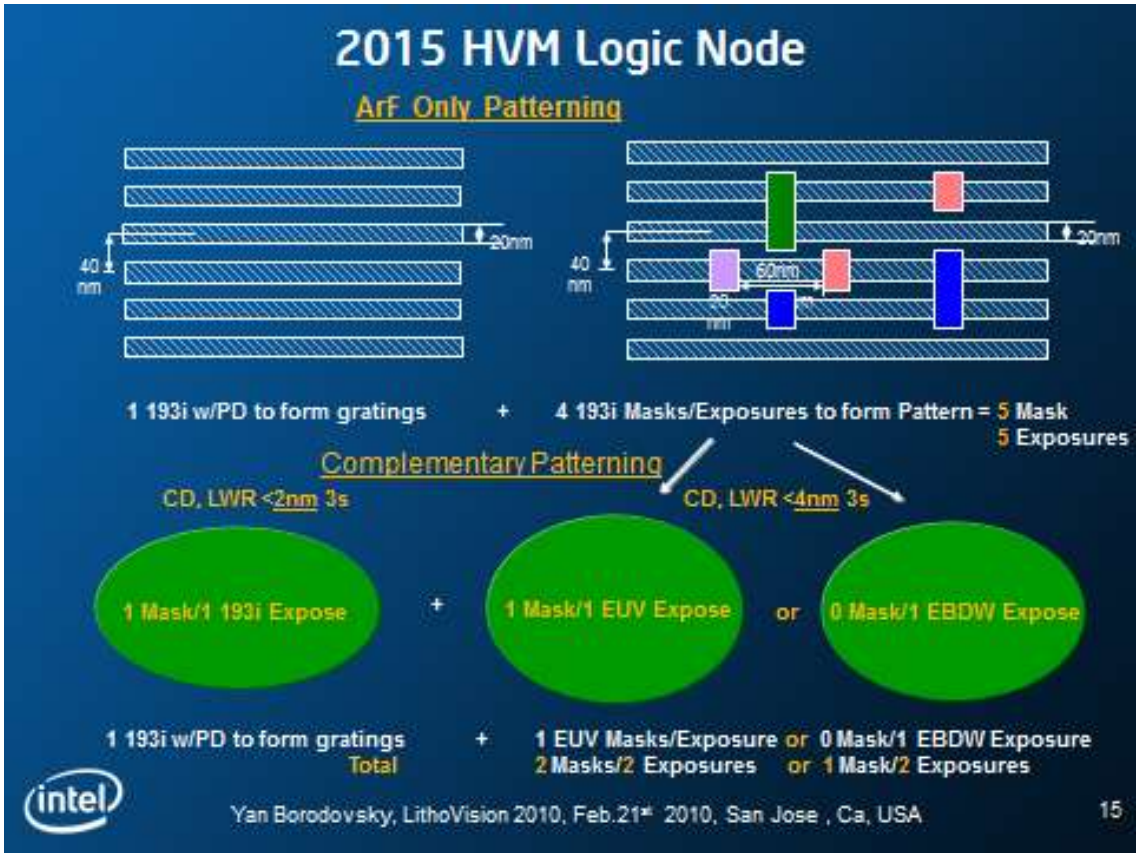


Complementary Patterning

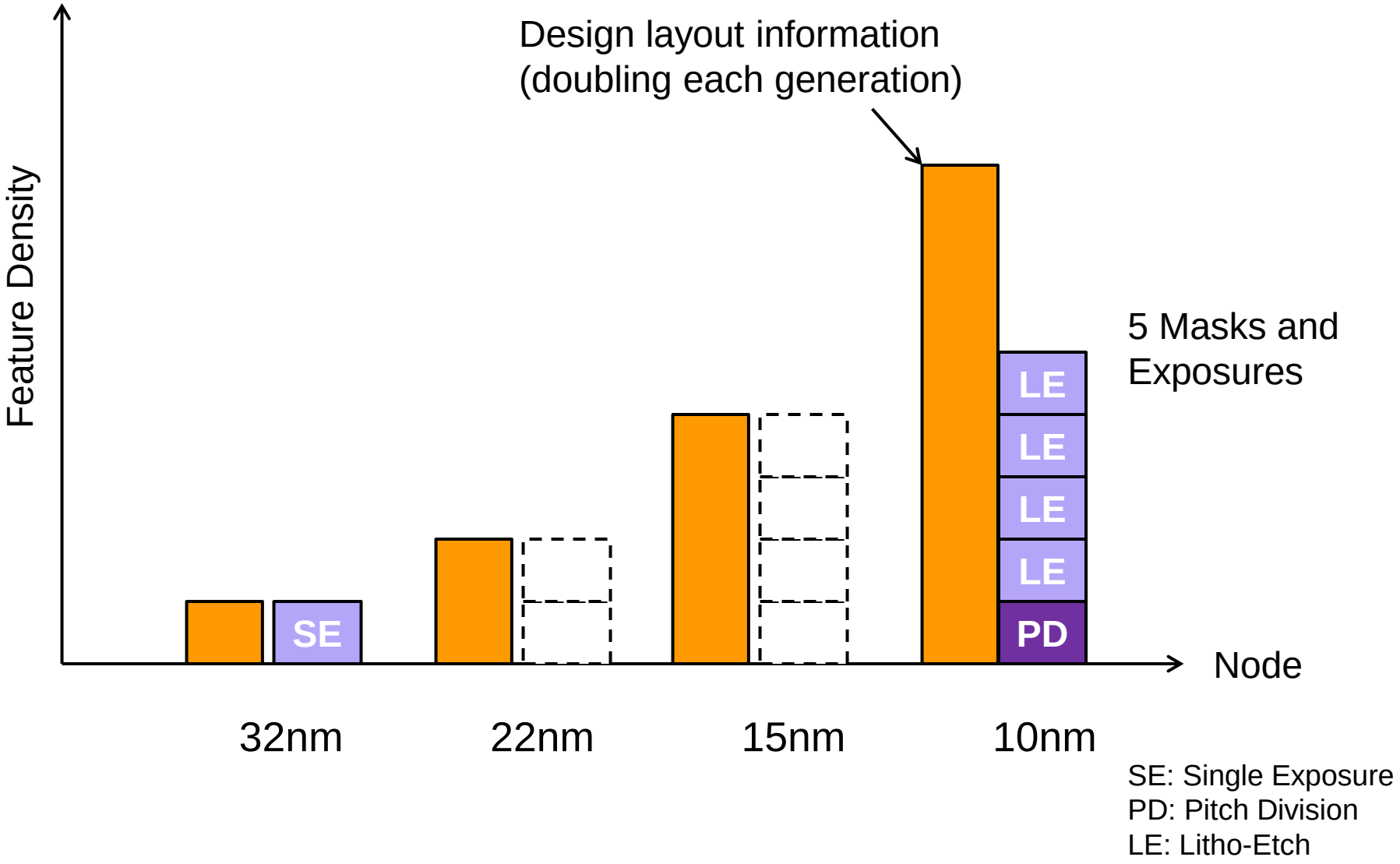
Not all exposures are equal

- ArFi + Spacer grating
- Cutting exposure alternatives:

1. ArFi-only patterning may require additional exposures to achieve needed density.
2. EUV single exposure
3. eBeam direct write. Low duty cycle of cutting pattern may enhance throughput

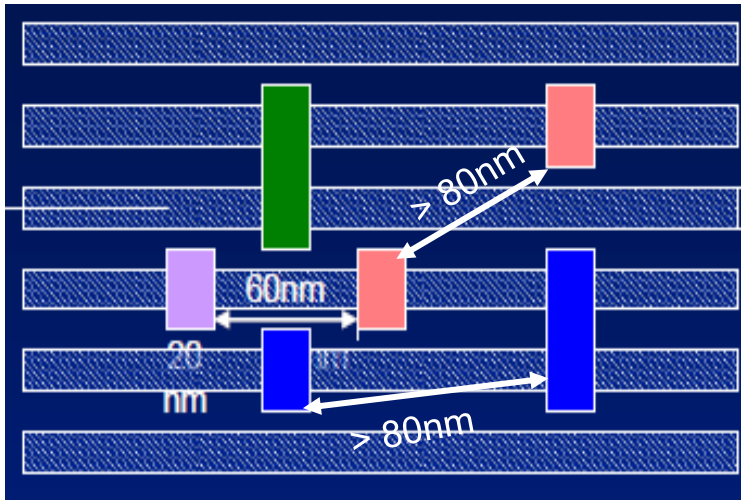


Complementary Patterning with ArF



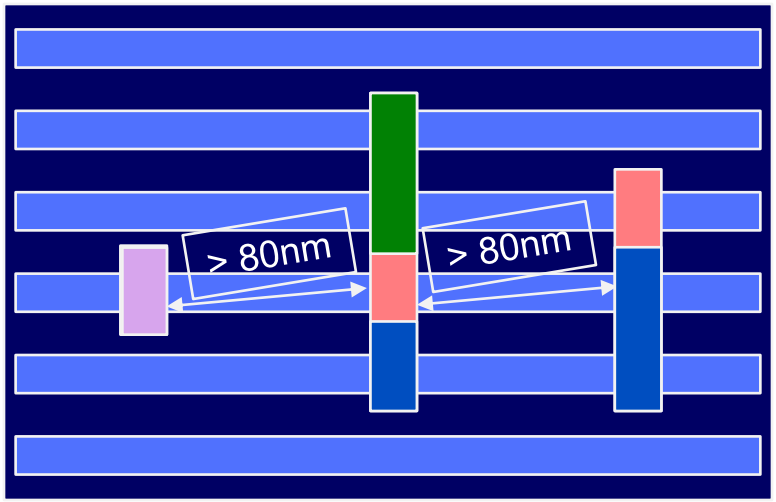
SE: Single Exposure
PD: Pitch Division
LE: Litho-Etch

More Design Constraints to Manage Cost…



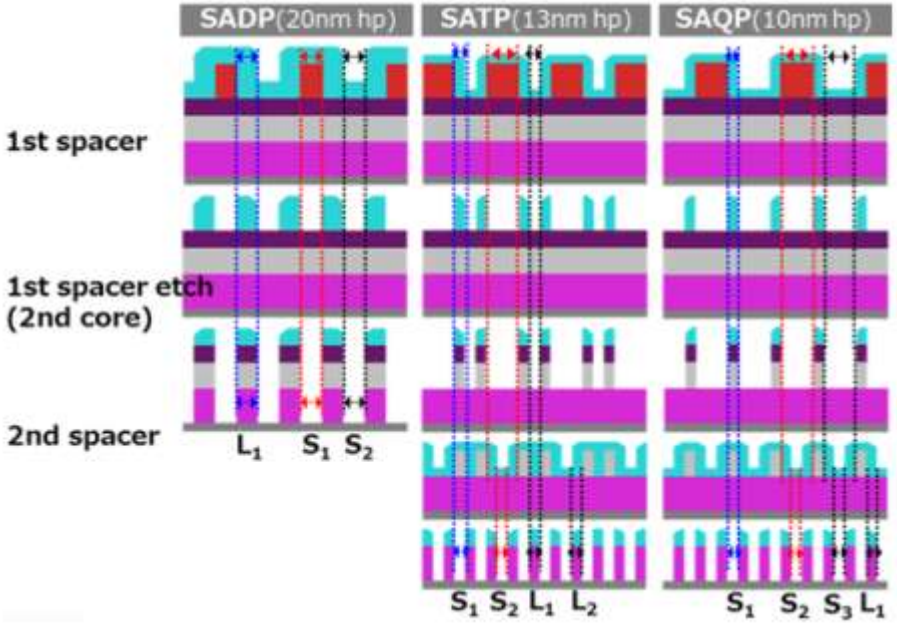
Using ArFi exclusively may result in five masks and exposures (2015 node)

Could the design layout be further constrained to minimize cut masks?

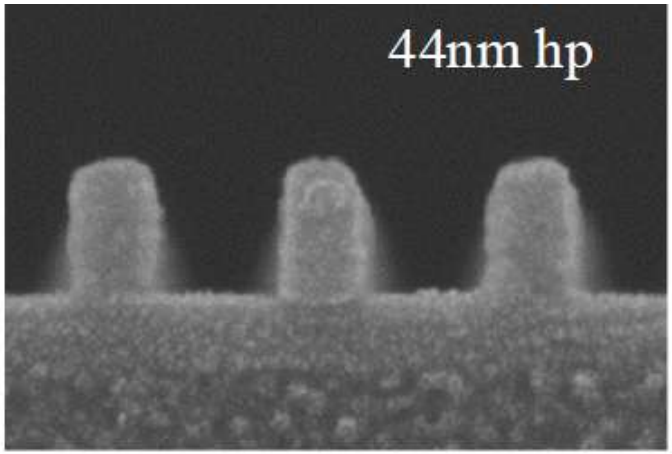


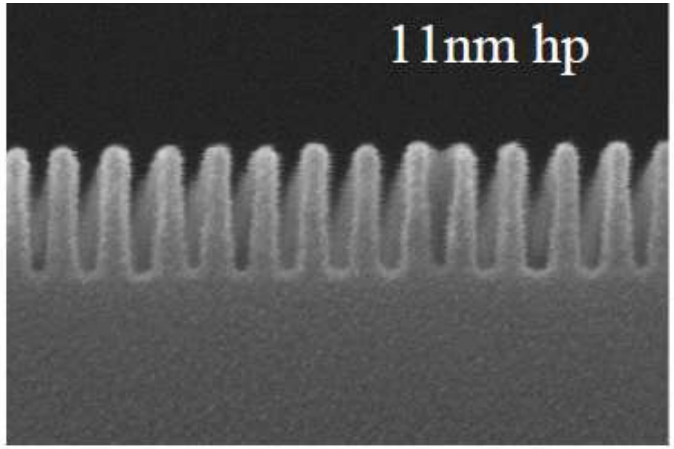
Ideally, by contemplating the cutting pattern in layout design, cuts could be grouped to conform to minimum pitch rules and fit onto fewer mask exposures.

Self-Aligned Quadruple Patterning (SAQP)



K. Oyama, *et al*, Tokyo Electron LTD
SPIE (2012) doi: 10.1117/12.916280

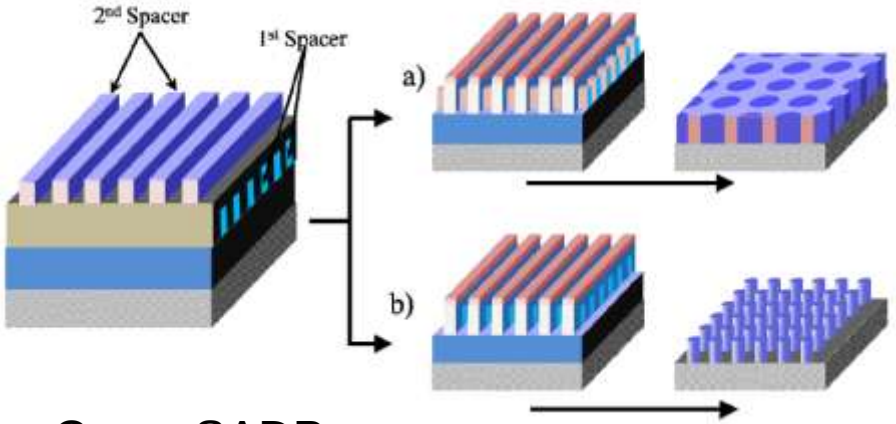




H. Yaegashi, *et al*, Tokyo Electron LTD
SPIE (2013) doi: 10.1117/12.2011962

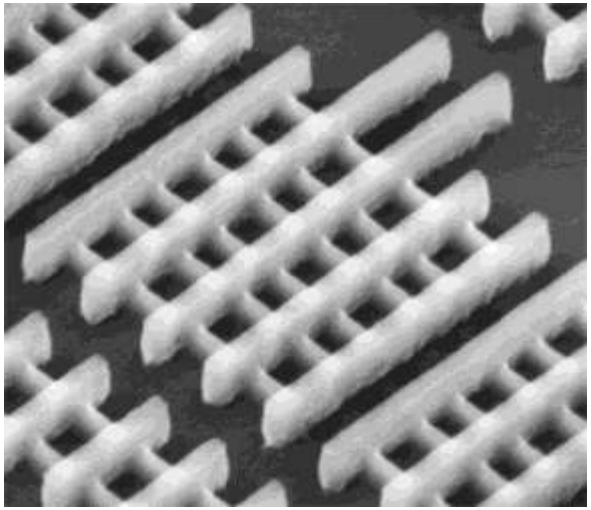
Compound Gratings

- 2X pitch division combined orthogonally can provide up to 4X feature density increase.
- For interacting process layers this 4X density could be achieved with a 2-3X increase in masks in the interacting layers.

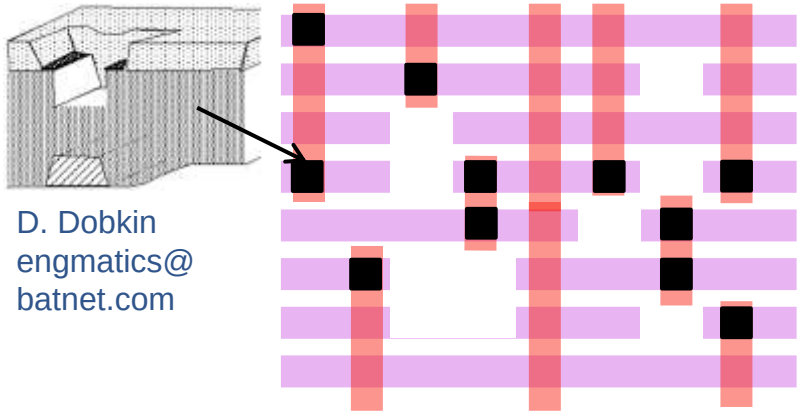


Cross-SADP process

S. Yamauchi, *et al*, Tokyo Electron LTD
SPIE (2013) doi: 10.1117/12.2011953



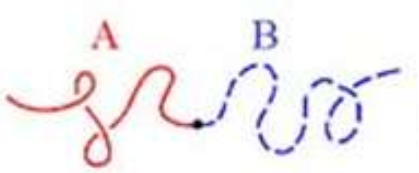
Intel 22nm FinFET



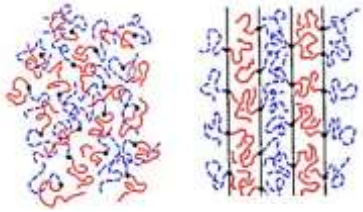
D. Dobkin
engmatics@
batnet.com

Self-aligned vias

Directed Self-Assembly (DSA) Pitch Division



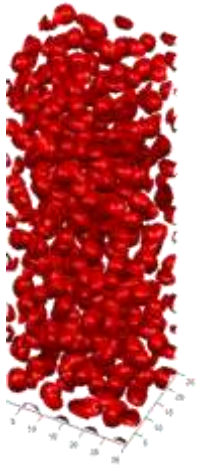
Di-block-copolymer molecule



lamellar

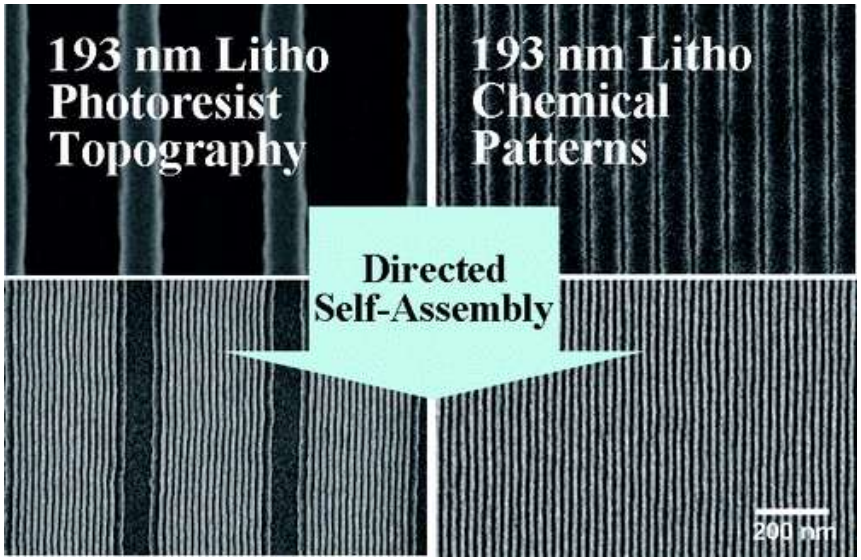
bicontinous
(gyroid)

cylinders

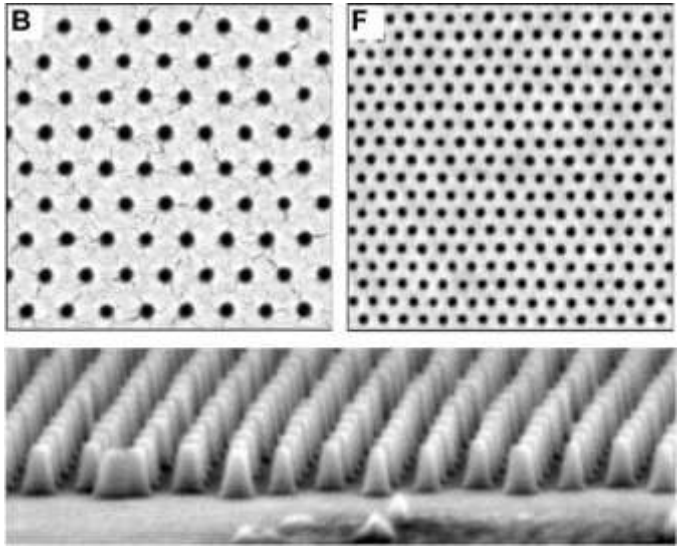


spheres

Synopsys prototype DSA simulator

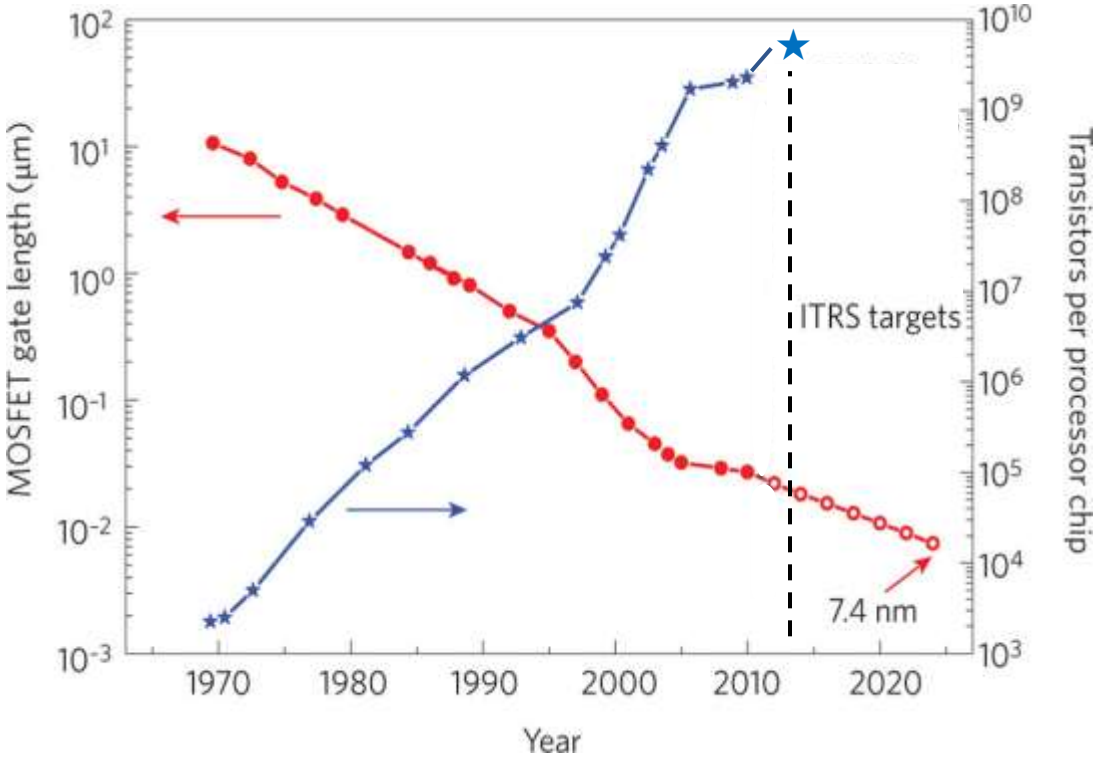


IBM, JSR Corp.



Paul Nealy, U. Wisonsin, Hitachi Global Storage Technologies

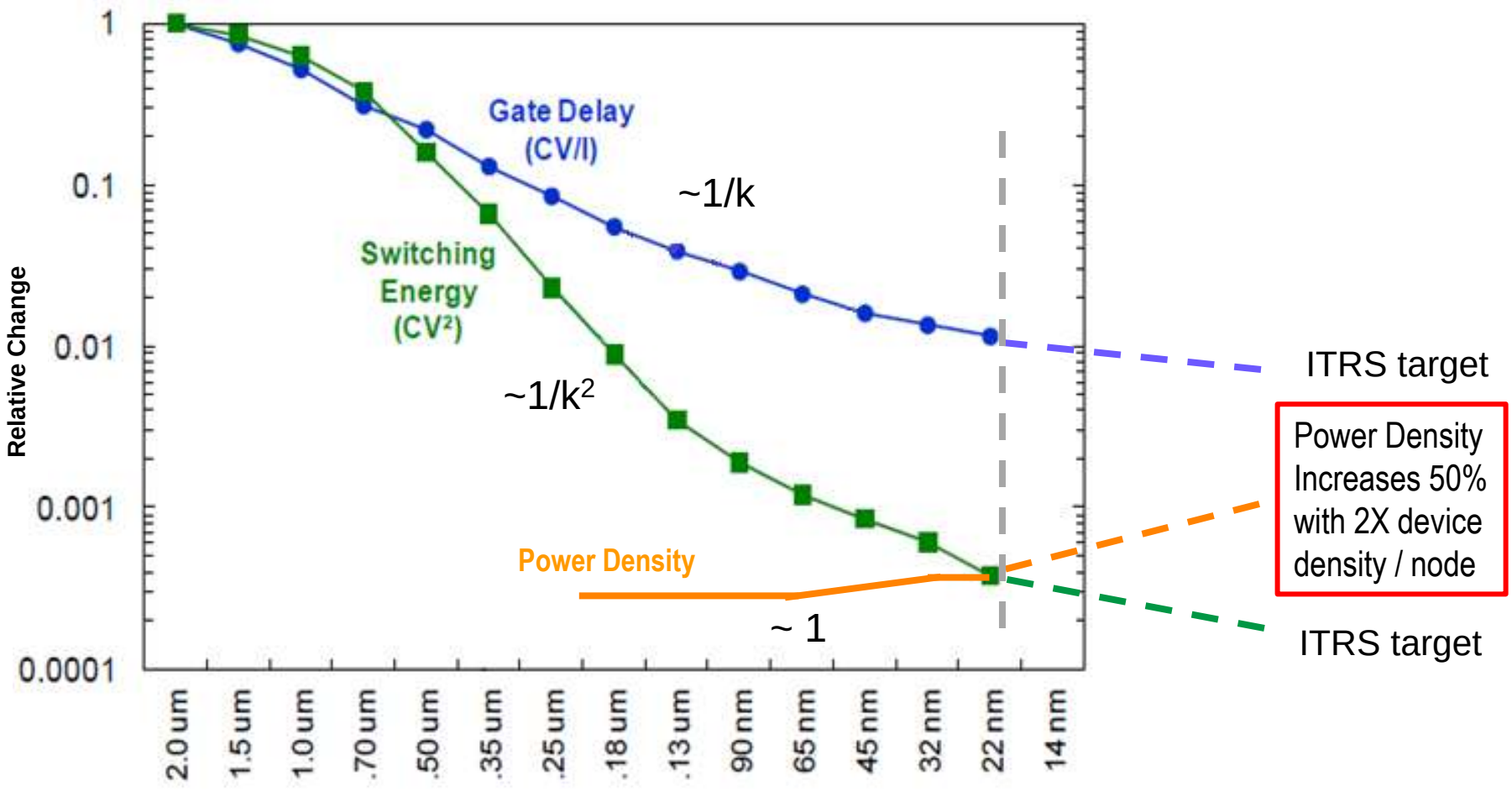
Dennard Scaling



Frank Schwierz, Nature Nanotechnology (2010)

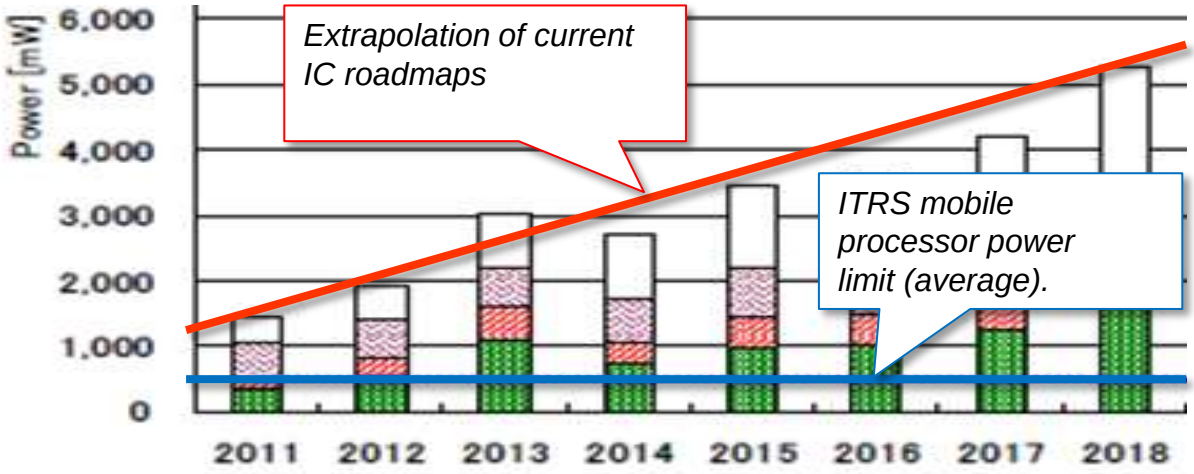
Dennard Scaling Device or Circuit Parameter	Scaling Factor
Device dimension D (t_{ox}, L, W)	1/k
Doping concentration N_a	k
Voltage V	1/k
Current I	1/k
Capacitance C	1/k
Delay CV/I	1/k
Power dissipation CV^2	1/k^2
Power density CV^2 / D^2	1

Device Scaling & Forecast (CMOS)

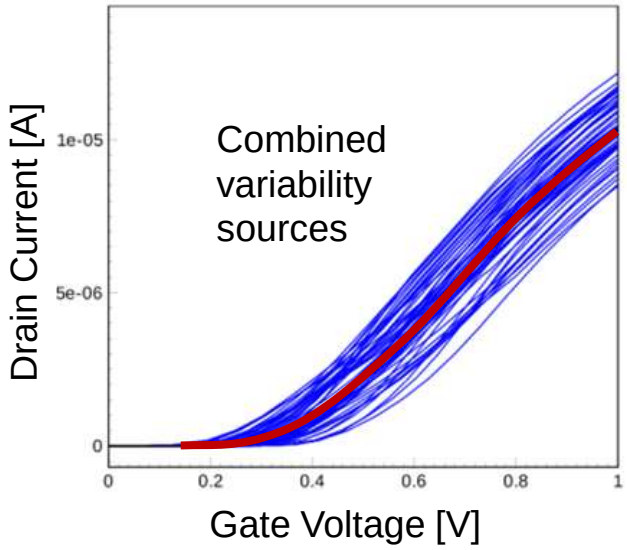


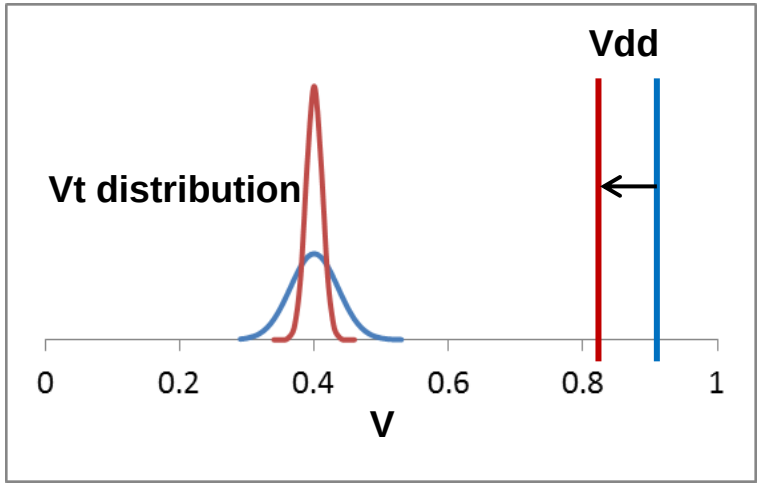
Mark Bohr, Intel

Variability and Power Efficiency

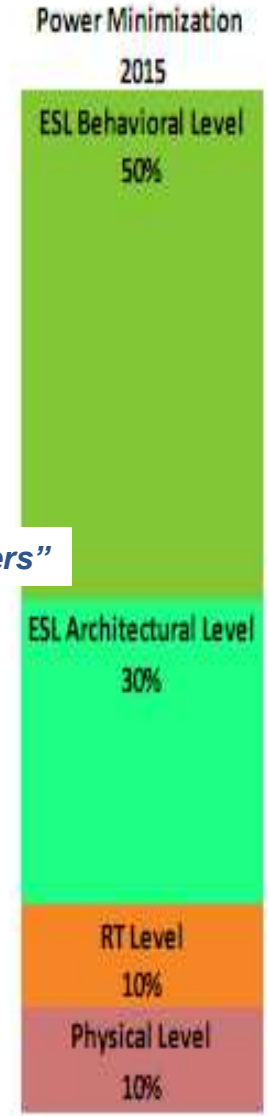


ITRS 2011 "System Drivers"



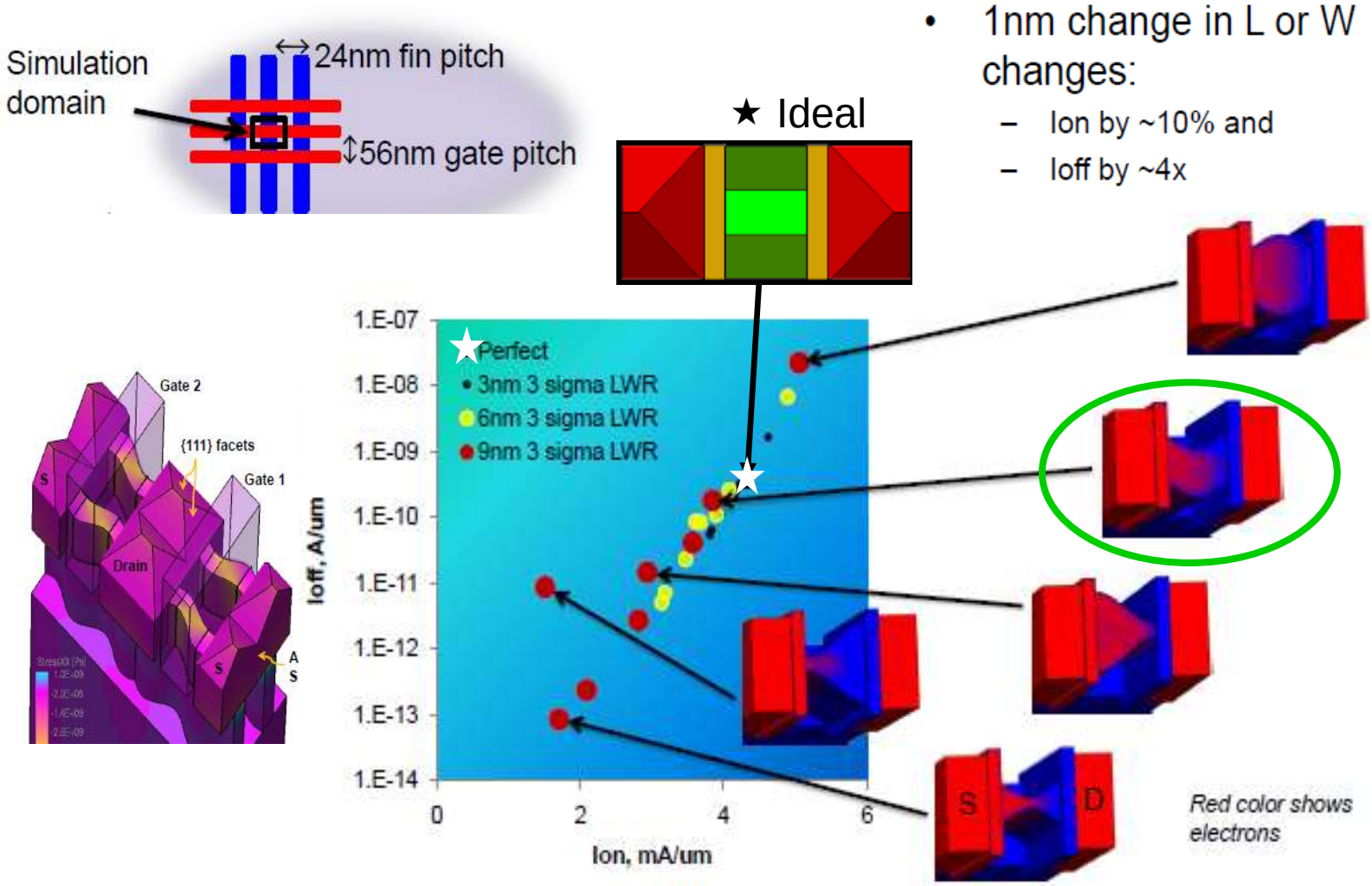


Reducing variability allows lower voltages and better power efficiency



Lithography processes that minimize patterning noise (eg LWR) have substantial value for power-efficient processes .

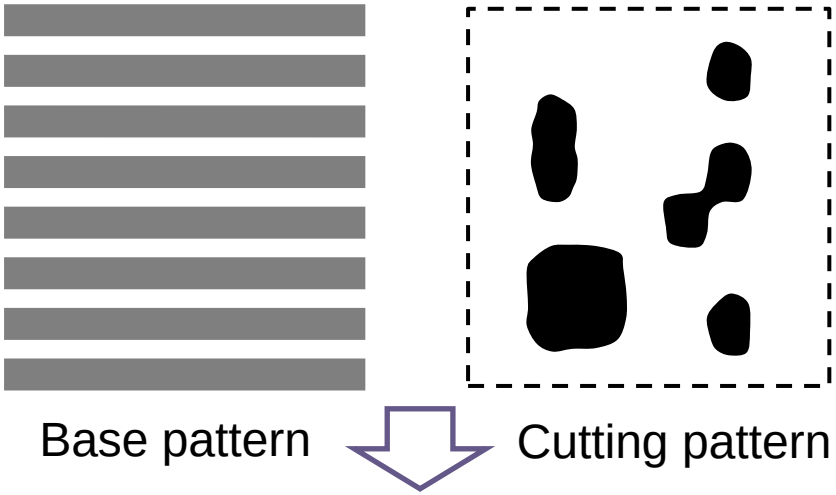
FinFET Electrical Variability with Pattern Variation



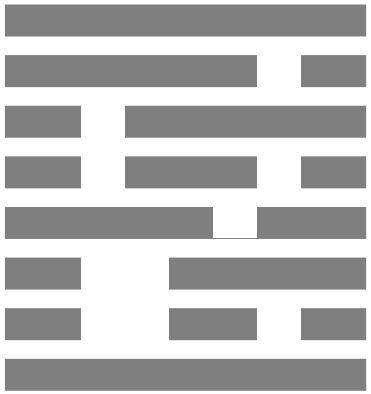
TCAD simulation demonstrates that variations in channel width have significant effects on transistor parameters, while variations on the path of the channel have minimal effect.

Minimizing Variability with Complementary Patterning

Uniform grating
- Fine pitch
- CD uniformity
- Low pattern flexibility

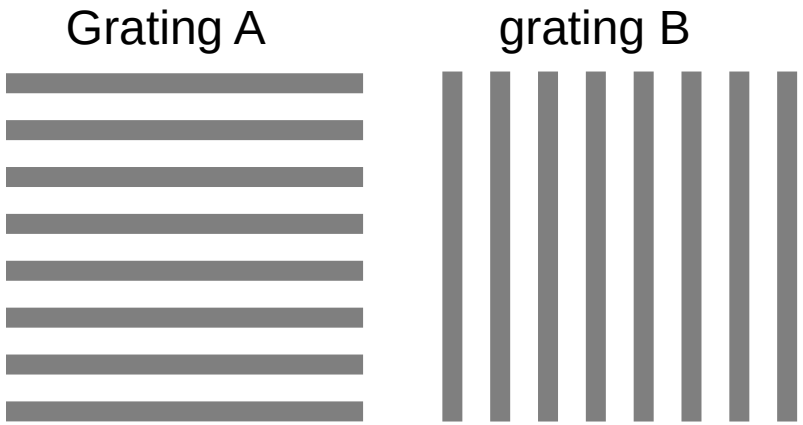


Cutting pattern defines line-ends only:
- High detail resolution
- Roughness less critical.
- Overlay margin = P/4.



Complementary patterning

Extending Complementary Patterning to Contacts



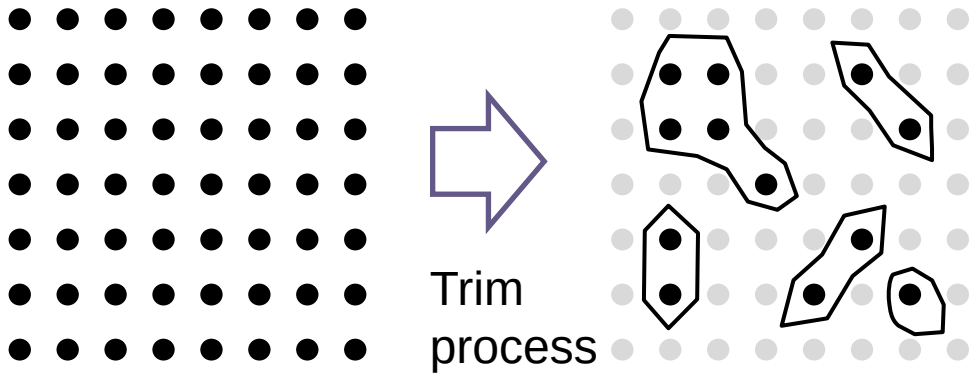
Trim pattern selects features to remain:

- ArF (193i) with a feature-shrinking process.
- EUV.
- eBeam direct write

Combining process

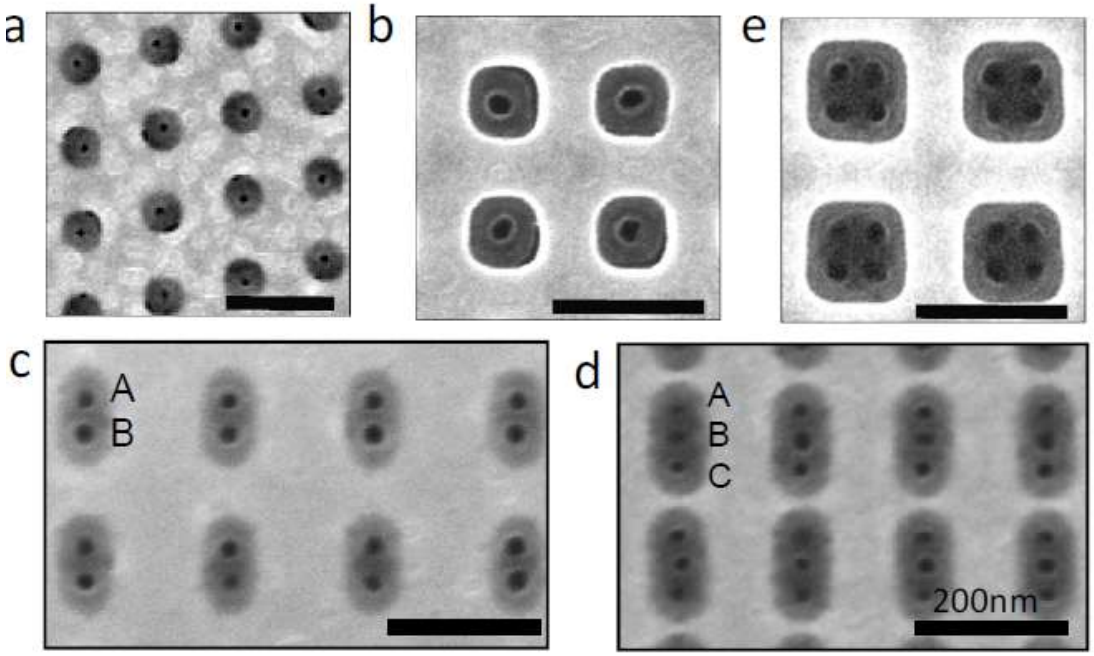
Trim Exposure

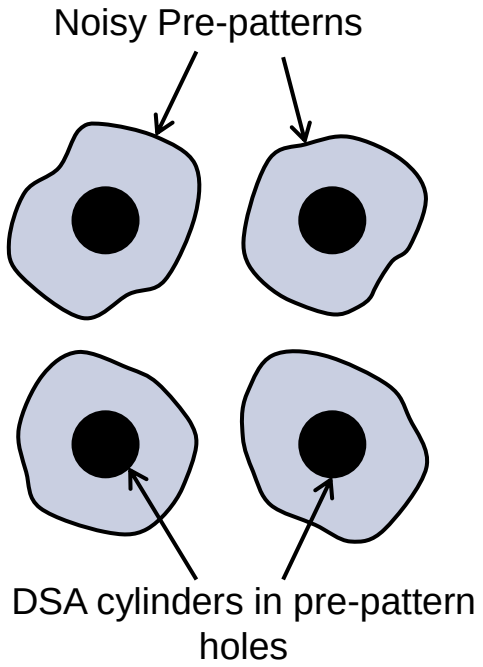
Or, use DSA cylinder array.



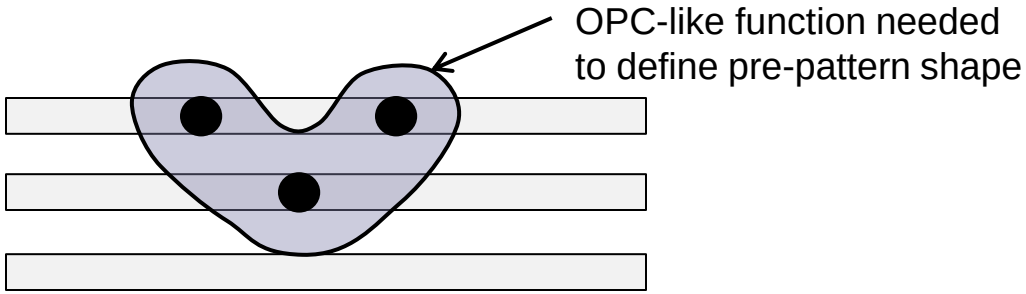
Trim process

DSA for contact holes





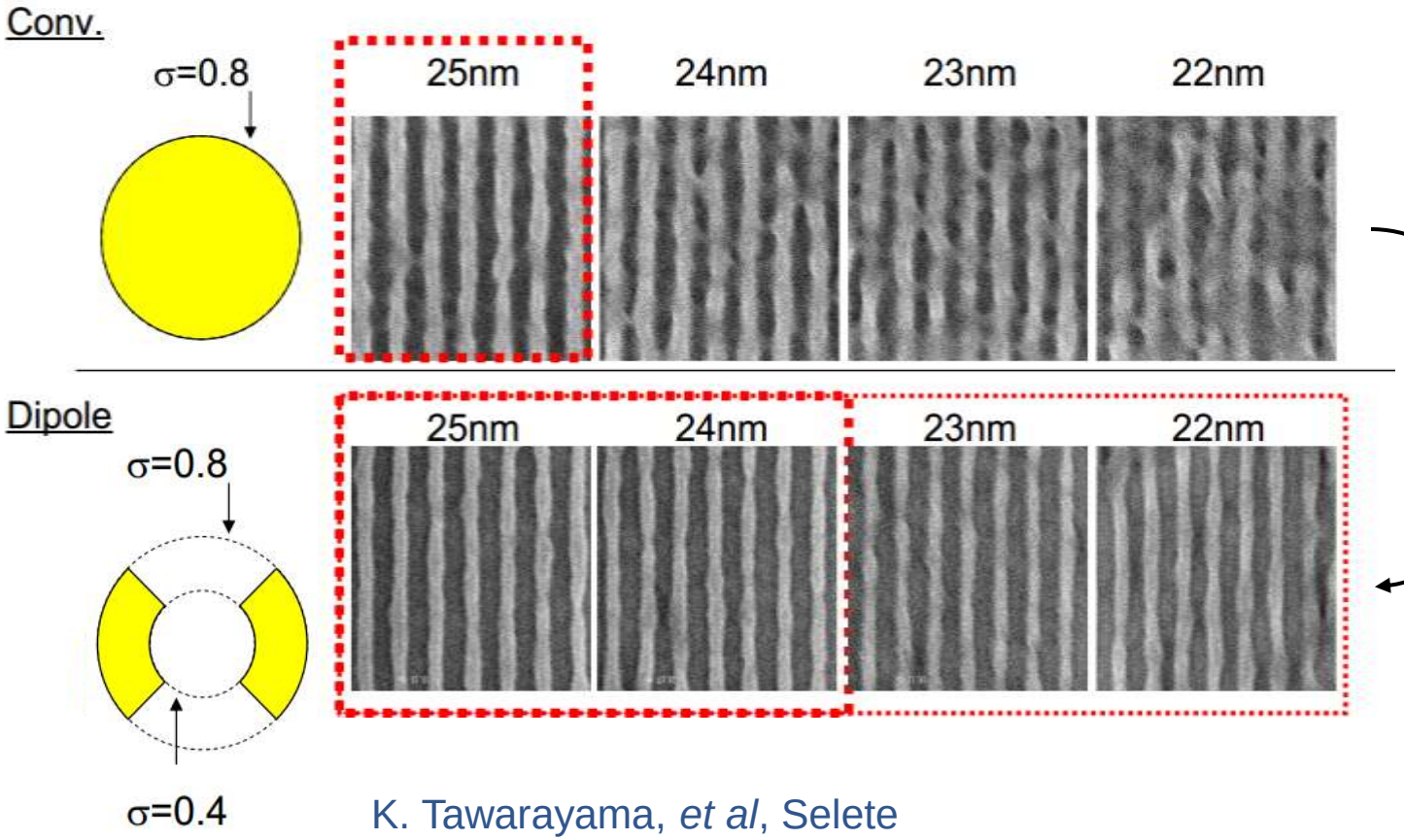
H-S Philip Wong, Chris Bencher, He Yi, Li-Wen Chang,
Block Copolymer Directed Self-Assembly Enables Sublithographic Patterning for Device Fabrication SPIE (2012) doi:10.1117/12.918312



Goals:

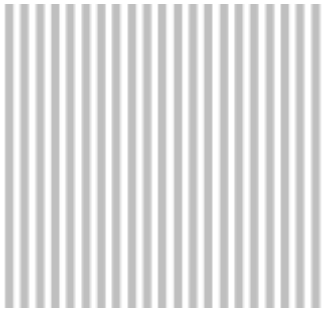
- Shrink features.
- Provide uniform CD.
- Improve placement error by averaging LER in pre-pattern
- Pitch division

Off-Axis Source Illumination for Reducing Pattern Variability

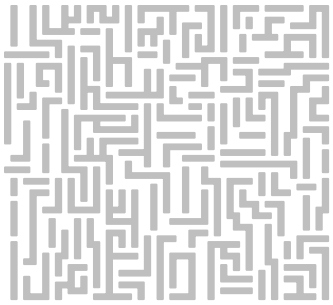


K. Tawarayama, *et al*, Selete
EUV Symposium 2009

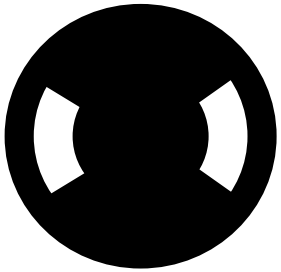
Source / Design Co-Optimization



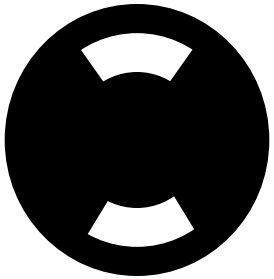
GRATINGS



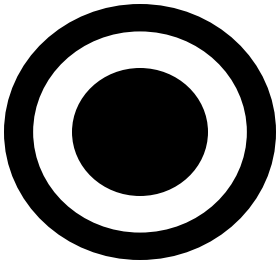
"RANDOM"



DIPOLE



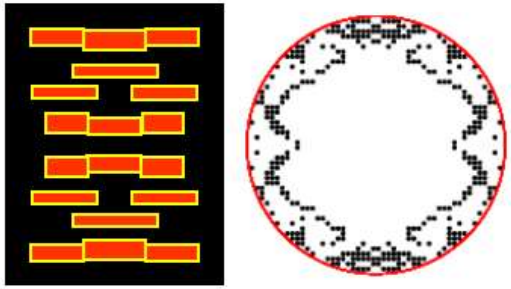
DIPOLE



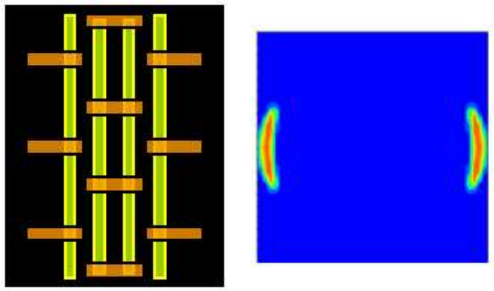
ANNULAR

The optical source (or pupilgram) can be customized for specific, regular design pattern configurations.

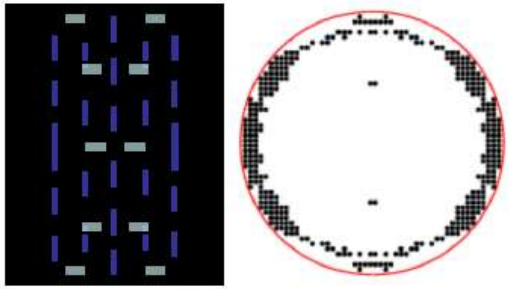
The trade-off is that many other pattern configurations do not image well, and they must be avoided in the design layout



ACTIVE



GATE

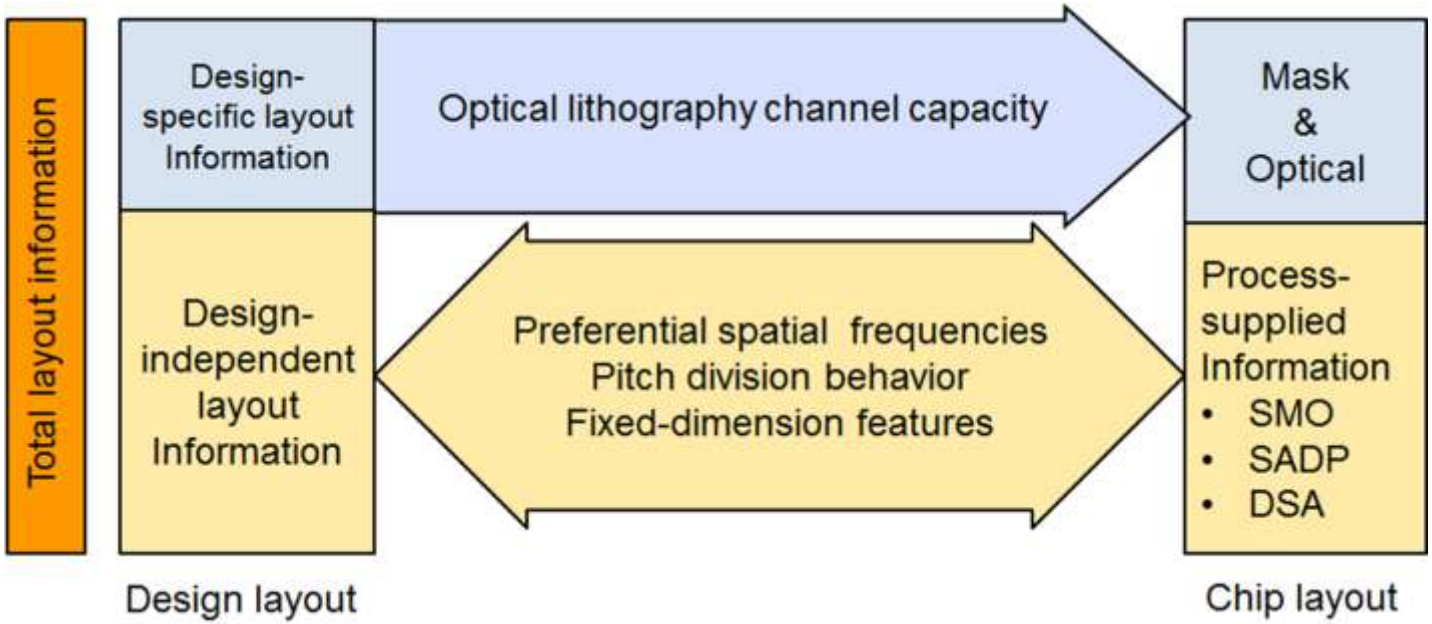


CONTACT

James Blatchford, TI, SPIE 2011

Summary

- For extending optical lithography for density, an increasing proportion of chip layout information is being supplied by the lithography process.



- To fully exploit these novel processes for density scaling, layout design and process co-optimization will be key.

Conclusions

- Extending chip density with precision detail for “More of Moore” is attainable, with or without EUV.
- The key challenge is to keep lithography costs under control.
  - Pitch division materials and process, such as Spacer and DSA, will be key.
  - But the penalty will be increasing loss of design layout flexibility.
- The best approach to advancing chip value is though design and process collaboration for balancing manufacturing cost with retaining essential degrees of freedom for effective layout design.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